

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Leonard Forbes et al.

Examiner: Son Dinh
Group Art Unit: 2824

Serial No.: Filed:

09/945,507 August 30, 2001

Docket: 1303.014US1

Title:

FLASH MEMORY WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS

COMMUNICATION CONCERNING RELATED APPLICATION(S)

MS RCE

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

Applicants would like to bring to the Examiner's attention the following related application(s) in the above-identified patent application:

<u>Serial/Patent No.</u> 09/945395	Filing Date August 30, 2001	Attorney Docket 1303.019US1	Title DRAM CELLS WITH REPRESSED FLOATING GATE MEMORY, LOW TUNNEL BARRIER INTERPOLY INSULATORS
09/943134	August 30, 2001	1303.020US1	PROGRAMMABLE ARRAY LOGIC OR MEMORY DEVICES WITH ASYMMETRICAL TUNNEL BARRIERS
09/945512	August 30, 2001	1303.027US1	IN SERVICE PROGRAMMABLE LOGIC ARRAYS WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS
09/945554	August 30, 2001	1303.028US1	SRAM CELLS WITH REPRESSED FLOATING GATE MEMORY, LOW TUNNEL BARRIER INTERPOLY INSULATORS
09/945500	August 30, 2001	1303.029US1	PROGRAMMABLE MEMORY ADDRESS AND DECODE CIRCUITS WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS
10/075484	February 12, 2002	1303.043US1	ASYMMETRIC BAND-GAP ENGINEERED NONVOLATILE MEMORY DEVICE
10/081818	February 20, 2002	1303.045US1	ATOMIC LAYER DEPOSITION OF METAL OXIDE AND/OR LOW ASYMMETRICAL TUNNEL BARRIER INTERPLOY INSULATORS

Serial Number: 09/945,507

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Title: FLASH MEMORY WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS

10/177096	June 21, 2002	1303.063US1	GRADED COMPOSITION METAL OXIDE TUNNEL BARRIER INTERPOLY INSULATORS
10/783695	February 20, 2004	1303.019US2	DRAM CELLS WITH REPRESSED FLOATING GATE MEMORY, LOW TUNNEL BARRIER INTERPOLY INSULATORS
10/781035	February 18, 2004	1303.063US2	GRADED COMPOSITION METAL OXIDE TUNNEL BARRIER INTERPOLY INSULATORS
10/788810	February 27, 2004	1303.027US2	IN SERVICE PROGRAMMABLE LOGIC ARRAYS WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS
10/819550	April 7, 2004	1303.019US3	DRAM CELLS WITH REPRESSED FLOATING GATE MEMORY, LOW TUNNEL BARRIER INTERPOLY INSULATORS

Respectfully submitted,

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<u>CERTIFICATE UNDER 37 CFR 1.8:</u> The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: MS RCE, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this <u>9th</u> day of <u>June</u>, 2004.

Name

Tina Kohul

Signature

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ATEMENT BY APPLICANT

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DATE CONSIDERED 3/5/04

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STATEMENT BY APPLICANT
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First Named Inventor

Group Art Unit

2824

Examiner Name

Dinh, Son

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT **Application Number** 09/945,507 August 30, 2001 Filing Date First Named Inventor Forbes, Leonard 2824 **Group Art Unit Examiner Name** Dinh, Son Attorney Docket No: 1303.014US1

	OTHER	R DOCUMENTS NON PATENT LITERATURE DOCUMENTS	
Examiner Initials*	Cite No 1	include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	۲
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